Roll No. | | | | | | | | | | |

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. / B. Tech / B. Arch (Full Time) - ARREAR EXAMINATIONS, APRIL/MAY 2024

ELECTRONICS AND COMMUNICATION ENGINEERING
Third Semester
EC7353 – DIGITAL ELECTRONICS AND SYSTEM DESIGN

(Regulation 2015)

Time: 3hrs

Max.Marks: 100

PART- A (10 x 2 = 20 Marks)
(Answer all Questions)

Q. No	Questions	Marks
1	Convert $(A2F)_{16}$ to decimal.	2
2	Prove the following: a) X(X'+Y) = XY b) X+XY = X	2
3	Draw a Full adder circuit using Half adder.	2
4	What are the applications of Encoder and Decoder.	2
5	Write down the characteristic equation and excitation table of JK flip flop.	2
6	What are shift registers?	2
7	What are races in asynchronous sequential circuits?	2
8	What are the different types of Hazards?	2
9	What is TTL logic? Mention it's types.	2
10	What is programmable logic array? How it differs from ROM?	2

PART- B (5 x 13 = 65 Marks)

Q. No	Questions	Marks
11 (a) (i)	State and Prove DeMorgan's Laws.	5
(ii)	Simplify the function using K map and Draw the Logic Circuit. X'Z'+WYZ+W'Y'Z'+X'Y	8
	(OR)	
11 (b)	Simplify the following Boolean function using Quine-McCluskey / Tabulation method. $F(A,B,C,D)= \sum(0,1,2,5,6,7,8,9,10,14)$	13
12 (a)	Design a Gray to Binary Code Converter circuit and Draw the logic diagram.	13
	(OR)	
12 (b) (i)	Draw the circuit diagram of Carry lookahead adder and explain.	8
(ii)	Draw the logic circuit diagram of 8 x 1 multiplexer.	5
13 (a)	Draw a SR Flipflop circuit and explain its operation with truth table. Mention the drawbacks of SR Flipflop and how to overcome it.	13
	(OR)	
13 (b)	Write short notes on: 1.Ring Counters 2.Ripple Counters	13
14 (a)	Obtain a reduced primitive flow table for an asynchronous sequential circuit with two inputs, A and B and one output, Z where Z changes whenever AB = 11. Assume that the two inputs do not change simultaneously and initial Z = 0.	13
	(OR)	

14 (b)	Write short notes on Essential Hazards. Explain in detail how to design a hazard free circuit.	13
15 (a) (i)	Explain the two input NAND and two input NOR gate realization using CMOS.	8
(ii)	Compare TTL and CMOS logic.	5
	(OR)	
15 (b)	Implement the following two Boolean functions with PLA and PAL: $F1$ = A'B+AC+A'BC' $F2$ = (AC+AB+BC)'	13

PART- C (1 x 15 = 15 Marks)

(Q.No. 16 is Compulsory)

Q. No	Questions	Marks
16	Design a sequential circuit with two D flip-flops A and B, and one input x_in, (a) When x_in = 0, the state of the circuit remains the same. When x_in = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats. (b) When x_in = 0, the state of the circuit remains the same. When x_in =1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeats.	15